ISSN:0975-9646

Low-Power 1-Bit Full-Adder Cell Using Modified Pass Transistor Logic

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Abstract: **Adders have become one of the important components in the digital world in such a way that there is no design without it. Adders are not only used for additions, but also used in many other functions like Subtractions, Multipliers, and Dividers etc. In the field of Very Large Scale Integration (VLSI), Adders are used as the basic component from processors to ASIC's. Hence a well optimized Adder design is needed. Propagation delay, Power and Area are the acceptable Quality metrics of the designed products. Recent days has proved that the use of Complementary Pass Transistor Logics (CPL) has provided a drastic reduction in the power compared to CMOS logic. This paper has spread the focus on Low power Adder design based on PTL's and achieved 2.5% reduction in power without affecting other quality metrics of the design. The design has been modelled and analyzed using TANNER EDA with TSMC MOSIS 250nm technology.**

Keywords: **Adder, Power, VLSI, CPL**

I. INTRODUCTION

The low-power VLSI demand can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level [1]. A proper logic style choice holds the key for the design and implementation of power efficient circuit systems, where the switching capacitance, transition activity, and short-circuit currents influences the power consumption. Among these parameters each plays their importance depending on the technique used in the circuit for the application.

Due to intent growth of the multimedia devices has made the Low power design as a major issue in modern world as opposed to past times parameters like high speed, small area and low cost. As a result many scientific communities associated with VLSI have turned their attention towards Low power design techniques. Most of the multimedia devices reliability has been reduced due to the mechanisms resulting in failure because of the power consumption. There are three major source of power consumption in CMOS VLSI circuits: 1) switching power due to charging and discharging of capacitances, 2) short circuit power due to current flow from power supply to ground with simultaneous functioning of p-network and n-networks, 3) static power due to leakage currents [2].

Literature review in the last decade has revealed some of the adder designs with different logic styles. In [1] Kang has proposed an adder design with pull-down and pull-up network using 28 transistors [3]. Full Adder using XOR/XNOR PTL cell with 16 transistors is reported in [4]. 32 Transistors Complementary pass-transistor logic (CPL) with high power dissipation and better driving capability was proposed in [5]. Full adder design with 10 transistors using XOR/XNOR gates is also reported in [6]. A hybrid CMOS logic style adder with 22 transistors is reported [7].

This paper is organized as follows. Section 2 describes the architecture of the full adder cell and provides the power optimized solution for the existing architecture of the literature. Simulation results and observations are discussed in section 3. Finally results are concluded and references are provided in sections 4 and 5 respectively.

II. FULL ADDER ARCHITECTURE

A basic full adder has three inputs and two outputs which are sum and carry. Full adder cell was designed with CPL and Multiplexing Control Input technique for both sum and carry operations. The Sum and Carry operations are based on the equations 1 & 2 mentioned below.

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = (A \oplus B)C + AB \quad (2)$$

Sum equation contains XOR gates whose design using CPL logic is desired for low power system, whereas the Carry is designed as per the equation.

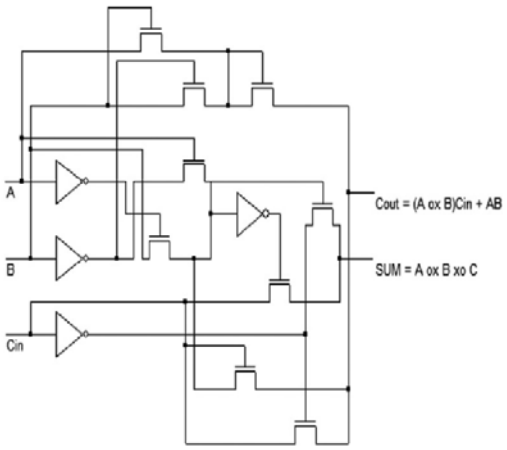

Fig 1: Full Adder Circuit [9]

The inputs *A*, *A*'s complement (*A*'), *B*, and *B*'s complement (*B*') are fed as inputs to the pass transistors and form an XOR logic gate. These four inputs construct an XOR logic operation at the transistor level, which is designed using two transistors. In order to reduce the number of transistors, the output of the XOR gate ($A \oplus B$) is fed through an NOT gate from the differential node to the pass transistors as a control input. On the other hand, C_{in} is treated as variable input, which is fed through the pass transistor source terminal. At

this stage, the functionality of the circuit is equivalent to the sum operation, sum $A \oplus B \oplus C$, and six transistors have been used. As mentioned before, the number of transistors in the carry operation can be reduced by taking $A \oplus B$ as the input from the sum operation circuit AND with C_{in} in order to produce the operation equivalent to $(A \oplus B)C_{in}$, which only uses another two transistors. Meanwhile, the inputs *A*, *A*', *B*, and *B*' are fed into pass transistors in order to produce an AND logic gate, which represents the *AB* operation in Equation (2). The outputs of both $(A \oplus B)$ *C* and *AB* are used as multiplexing inputs in order to sum both terms with the OR gate operation. The transistor count can be reduced by modifying the OR gate at the last stage of the carry equation. This is done by removing the inverter and the transistor fed by the inverter. Markovic's [8] full adder circuit has 22 transistors. At an earlier point, 3 transistors were omitted in our design and the number of transistors of the full adder cell was reduced to 17 transistors, which is lower than the number of transistors in the circuit described by Markovic [8] which is 22. Fig 1 shows the full adder circuit using 17 transistors [9]. And Fig 2 shows the proposed full adder circuit for power optimization.

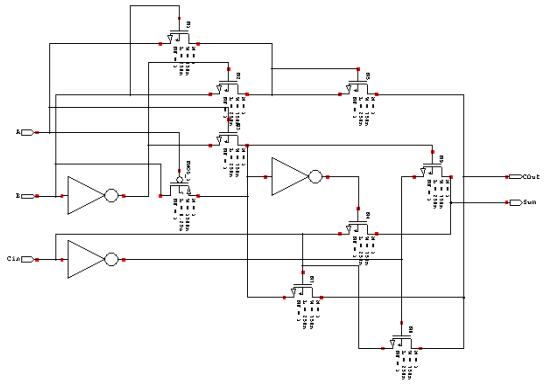

Fig 2. Proposed Full Adder circuit

The proposed low power full adder consists of both PMOS & NMOS transistors. The innovation is in eliminating the power hungry inverters. The NMOS transistors that require inversion of gate input has been replaced by PMOS transistors.

III. SIMULATION AND PERFORMANCE ANALYSIS OF FULL ADDER

The existing & proposed architectures are implemented using Full Custom AISC design methodologies. Both the existing & proposed full adder architectures were simulated using Tanner tool which are mapped to TSMC 250 nm technology node.

The Table I shows the benchmarking results of the existing & proposed architectures after implementing using ASIC design methodology. As depicted in Table I the proposed architecture is well suited for area optimized applications and the performance of the proposed architecture is also unaffected. From Table I, it is clear that the proposed architecture out performs the existing architecture in all the design aspects (Area & Power). It is interesting to note that power has been reduced. Since it is an architectural innovation, below are the low power advantages:

- No Area or Performance penalty.
- Minimum Verification effort:
  - Since it is correct by design.
- It is pervasive:
  - It is independent of adder width.
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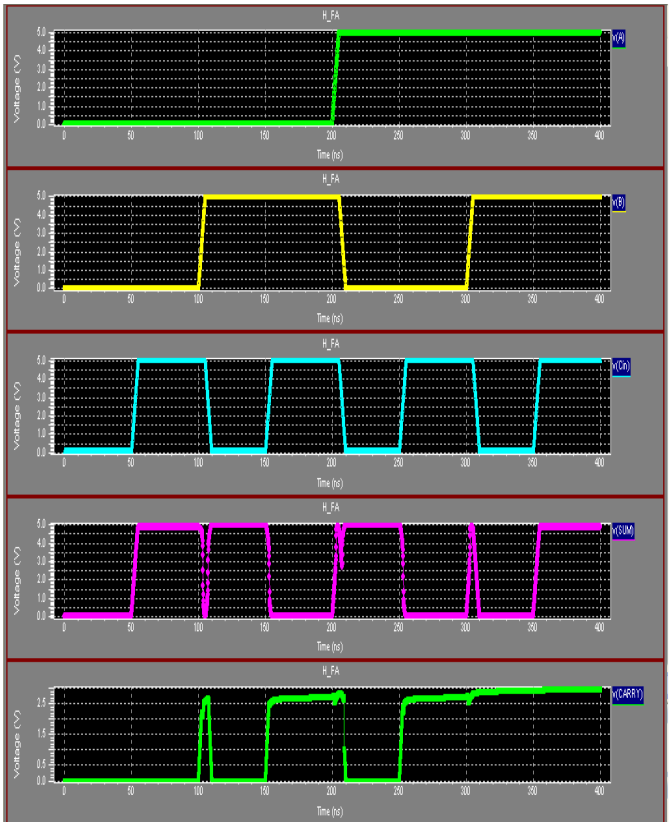

Fig 3: Waveforms of the Full Adder

Table 1: Benchmarking results @3.3V

Module	Existing Architecture	Proposed Architecture	Percentage Gain
Full Adder	A = 17 T = { A to sum = 225.78 A to carry = 173.28} P= 205.072	A = 15 T = { A to sum = 225.73 A to carry = 173.23} P= 200.042	A = 11% P = 2.5%

Note:

A = Area in transistor count
T = Delay in ns.
P = Power in nW.

IV. CONCLUSION

The proposed full adder cell has been simulated and results are compared with existing full adder cell in terms of power and delay. This proposed adder cell is having improvement in both of these aspects. The proposed low power concept is proven in both ASIC Design Methodologies.

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